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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,176	12/04/2001	Edward Benyukhis	CE08625I	2846

22917 7590 04/23/2004

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EXAMINER	
CHEN, ALAN S	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 04/23/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

7

Office Action Summary	Application No.	Applicant(s)	
	10/006,176	BENYUKHIS ET AL.	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/04/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by No. 6,567,912 to Belkin et al. (hereafter Belkin).

3. As per claims 1 and 8, Belkin discloses a method and system for improved initialization of a high availability system (Fig. 1, element 1) that comprises a controller component and a plurality of peripheral components (Fig. 1, element 112, 114 and 116), the method and system comprising:

applying power by a controller component (Fig. 6, element 105) to a first peripheral component (Fig. 1, element 118 and Fig. 2, element 206, the controller component boots/powers up the first device on the list, e.g., book program device #1).

when initialization of the first peripheral component is received by controller component storing an identifier of the first peripheral component (Fig. 1, element 126, where identifier is indicates whether initialization passed or failed); applying power (e.g., booting) by the controller component to a next peripheral component (Fig. 2, element 212).

when the first peripheral component, while initializing, locks up the bus that the controller component and the plurality of peripheral devices share (when watch-dog timer

expired, Fig. 2, element 216), restarting the power-up sequence (Fig. 2, element 228, attempt to reboot failed device); determining that an identifier of the first peripheral component was not stored (e.g., had a failed status, and not storing the pass status) and skipping first peripheral component that failed (it can be seen in Belkin, Fig. 2, that if the device failed twice to initialize then there is no procedure after the second failure to attempt to initialize the device again, and hence, the device is left as failed. It would clearly not be logical for the device to constantly be rebooted if it has failed twice already, since this would consume much time on the bus).

4. As per claims 2 and 9, Belkin discloses the method and system of claims 1 and 8, respectively, wherein restarting the power-up sequence comprises reinitializing the high availability system (Fig. 2, element 228, act of rebooting is equivalent to reinitialization where the state machine of the system started at its initial state).

5. As per claims 3 and 10, Belkin discloses the method and system of claims 2 and 9, respectively, further comprising the step of both expiring by a watchdog timer (Fig. 2, element 216) and triggering the re-initialization of the high availability system (Fig. 2, element 226), when the first peripheral component locks up the bus (note that the first peripheral component of Belkin can clearly have the potential to LOCK up. Belkin invention of robust initialization is to deal with any device that locks up).

6. As per claims 4 and 11, Belkin discloses the method and system of claims 2 and 9, respectively, wherein storing comprises storing the identifier in a memory device whose contents survive a reinitialization of the high availability system (the identifier PASS and FAIL, Fig. 1, elements 126 and 136 are the result of surviving a reinitialization, Fig. 2, element 226, e.g., if the device failed the reinitialization again, then it is still marked with a "FAILED" status. Also, the

boot marker (Fig. 1, element 120, is also an identifier indicating which device to boot next, stored in the memory device).

7. As per claims 5 and 12, Belkin discloses the method and system of claims 4 and 11, respectively, wherein the memory device comprises a non-volatile random access memory (Fig. 1, element 108).

8. As per claims 6 and 13, Belkin discloses the method and system of claims 1 and 8, respectively, wherein storing comprises storing a value in a location in a memory array (Fig. 1, element 108) that corresponds to the first peripheral component (Fig. 1, element 122).

9. As per claims 7 and 14, Belkin discloses the method and system of claims 6 and 14, respectively, wherein clearing the contents of the location in the memory array corresponds to the first peripheral component prior to the step of applying power to the first peripheral component (this case is anticipated by Belkin by his boot marker, Fig. 1, element 120. In Fig. 2, element 222, it can be seen that the boot marker is erased and updated prior to the power on of the device that the updated boot marker is pointing to. This makes sense since the controller always will need to know which device to power on before it can actually apply the power).

Response to Arguments

10. Applicant's arguments, see applicants amendment, filed 12/4/2003, with respect to the rejection(s) of claim(s) 1-14 under 35 U.S.C. 102(b) and 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of No. 6,567,912 to Belkin et al.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
04/21/2004

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100